IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) A sigma delta interpolator for use in a fractional N synthesizer having a multi-modulus divider, said sigma delta interpolator comprising:

an accumulator operative for receiving an input signal representing a desired frequency output of said fractional N synthesizer and for generating a digital output signal having M bits, which include N most significant bits and n least significant bits, said N most significant bits being coupled to said multi-modulus divider and operative for controlling the operation of said multi-modulus divider; and

a delay circuit coupled to said accumulator, said delay circuit receiving said n least significant bits and operative for implementing a delay function defined by equation: $1-(1-Z^{-1})^N$,

wherein N corresponds to the order of the sigma delta interpolator, and N is greater than or equal to 2.

2. (Original) The sigma delta interpolator for use in a fractional N synthesizer having a multi-modulus divider according to claim 1, wherein said sigma delta interpolator is a fourth order sigma delta interpolator.

3. (Original) The sigma delta interpolator for use in a fractional N synthesizer having a multi-modulus divider according to claim 2, wherein said digital output signal of said accumulator comprises a 32 bit word, with the 4 most significant bits of said 32 bit word being coupled to said multi-modulus divider and the 28 least significant bits of said 32 bit word being coupled to the said delay circuit.

4. (Original) The sigma delta interpolator for use in a fractional N synthesizer having a multi-modulus divider according to claim 1, wherein said N most significant bits output by said accumulator correspond to said desired frequency output of said fractional N synthesizer.

5. (Original) The sigma delta interpolator for use in a fractional N synthesizer having a multi-modulus divider according to claim 4, wherein said accumulator is the sole accumulator utilized in said sigma delta interpolator.

6. (Original) The sigma delta for use in a fractional N synthesizer having a multi-modulus divider according to claim 4, wherein said N most significant bits output by said accumulator and coupled to said multi-modulus divider are the sole control signals received by said multi-modulus divider the effect the desired output frequency generated by said fractional N synthesizer.

7. (Currently amended) A sigma delta interpolator for use in a fractional N synthesizer having a multi-modulus divider, said sigma delta interpolator comprising:

an accumulator operative for receiving an input signal representing a desired frequency output of said fractional N synthesizer and for generating a digital output signal having M bits, which include N most significant bits and n least significant bits, said N most significant bits being coupled to said multi-modulus divider and operative for controlling the operation of said multi-modulus divider; and

a delay means coupled to said accumulator, said delay means receiving said n least significant bits and operative for implementing a delay function defined by equation: $1-(1-Z^{-1})^N$,

wherein N corresponds to the order of the sigma delta interpolator, and N is greater than or equal to 2.

8. (Original) The sigma delta interpolator for use in a fractional N synthesizer having a multi-modulus divider according to claim 7, wherein said sigma delta interpolator is a fourth order sigma delta interpolator.

9. (Original) The sigma delta interpolator for use in a fractional N synthesizer having a multi-modulus divider according to claim 8, wherein said digital output signal of said accumulator comprises a 32 bit word, with the 4 most significant bits of said 32 bit word being coupled to said multi-modulus divider and the 28 least significant bits of said 32 bit word being coupled to the said delay means.

10. (Original) The sigma delta interpolator for use in a fractional N synthesizer having a multi-modulus divider according to claim 7, wherein said N most significant bits output by said accumulator correspond to said desired frequency output of said fractional N synthesizer.

11. (Original) The sigma delta interpolator for use in a fractional N synthesizer having a multi-modulus divider according to claim 10, wherein said accumulator is the sole accumulator utilized in said sigma delta interpolator.

12. (Original) The sigma delta for use in a fractional N synthesizer having a multi-modulus divider according to claim 10, wherein said N most significant bits output by said accumulator and coupled to said multi-modulus divider are the sole control signals received by said multi-modulus divider the effect the desired output frequency generated by said fractional N synthesizer.

13. (Currently amended) A fractional N frequency synthesizer comprising:

a sigma-delta interpolator including an accumulator operative for receiving an input signal representing a desired frequency output of said fractional N synthesizer and for generating a digital output signal having M bits, which include N most significant bits and n least significant bits, and a delay circuit coupled to said accumulator, said delay means receiving said n least significant bits and operative for implementing a delay function defined by equation: $1-(1-Z^{-1})^N$, and

a phase-lock loop circuit comprising a voltage controlled oscillator for generating a carrier signal and a programmable frequency divider, said programmable frequency divider receiving said N most significant bits as an input signal, said programmable frequency divider operative for changing the frequency of the carrier signal in accordance with said N most significant bits,

wherein N corresponds to the order of the sigma delta interpolator, and N is greater than or equal to 2.

14. (Original) The fractional N synthesizer according to claim 13, wherein said sigma delta interpolator is a fourth order sigma delta interpolator.

15. (Original) The fractional N synthesizer according to claim 14, wherein said digital output signal of said accumulator comprises a 32 bit word, with the 4 most significant bits of said 32 bit word being coupled to said multi-modulus divider and the 28 least significant bits of said 32 bit word being coupled to the said delay means.

16. (Original) The fractional N synthesizer according to claim 13, wherein said N most significant bits output by said accumulator correspond to said desired frequency output of said fractional N synthesizer.

17. (Original) The fractional N synthesizer according to claim 16, wherein said accumulator is the sole accumulator utilized in said sigma delta interpolator.

18. (Original) The fractional N synthesizer according to claim 16, wherein said N most significant bits output by said accumulator and coupled to said programmable frequency divider are the sole control signals received by said programmable frequency divider that effect the desired output frequency generated by said fractional N synthesizer.